(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **08235878 A**
(43) Date of publication of application: **13.09.1996**

(51) Int. Cl **G11C 16/06**
H01L 27/115

(21) Application number: **07038576**
(22) Date of filing: **27.02.1995**

(71) Applicant: **HITACHI LTD**
(72) Inventor: **KINO YUSUKE**
KAWAHARA TAKAYUKI
KIMURA KATSUTAKA

(54) NONVOLATILE SEMICONDUCTOR STORAGE

(57) Abstract:

PURPOSE: To continuously read out information of a memory array at high speed by selectively controlling respective blocks consisting of plural bit line pairs and latch circuits of the same number as that of bit line pairs.

CONSTITUTION: A memory mat is constituted by being divided into a bank A and a bank B. Bit lines BL11a to na of the bank A and bit lines BL11b to nb at the bank B become pairs to share sense-latch circuits SL11 to 1n, SL n1 to n4. Respective bit line information are alternately latched in a circuit SLa by switches YS1a, YS2a of the double period operations of an external clock via subinput-output lines IO1a, IO2a from circuits SL11 to 14 temporarily holding block memory cell information of bit lines BL11a to 14a connected to the word line W1 of the memory array MAa of the bank A to be outputted to a line IOa in synchronization with the clock by a switch SWa. After the readout, circuits SL11 to 14 are reset and bit lines of the B side are precharged during the outputting of the bank A and then information are read out continuously by alternately rising up word lines of the bank A and the bank B.